WHAT IS CLAIMED IS:

1. An apparatus for reading data from a disk, wherein the data is recorded in a data portion provided in each sector on the disk based on address information recorded in a header portion provided in that sector, the apparatus comprising:

a read clock generating circuit for generating a read clock signal based on rotational speed and recording density of the disk.

2. The apparatus according to claim 1, wherein the disk has a plurality of zones where data is recorded in those zones at different recording densities and the read clock generating circuit includes an arithmetic operation circuit for computing a frequency of the read clock signal in accordance with the rotational speed of the disk and the recording density of each zone.

3. The apparatus according to claim 1, wherein the disk has a plurality of zones where data is recorded in those zones at different recording densities, a frequency of the read clock signal differs zone by zone, and the read clock generating circuit includes a memory where a table of frequencies of a plurality of read clock signals associated with the plurality of zones is stored.

4. The apparatus according to claim 1, further comprising an ID reading apparatus which operates in accordance with the read clock signal to read the address information and the data.

5. The apparatus according to claim 1, further comprising:

a first delay circuit for generating from the read clock signal a first delay clock signal delayed by a predetermined phase from the read clock signal; and

a second delay circuit for generating from the read clock signal a second delay clock signal delayed by the predetermined phase from the first delay clock signal.

6. An apparatus for reading data recorded on a disk having sectors with each sector including a header portion having an address sync mark and address information and a data portion where the data is recorded, the apparatus comprising:

a read clock generating circuit for generating a read clock signal based on a rotational speed and recording density of the disk;

a first ID reading apparatus which operates in accordance with the read clock signal, the first ID reading apparatuses including:

a first address sync mark detection circuit for detecting the address sync mark from data read from the header portion in accordance with the read clock signal and generating an address sync mark detection signal;

a first ID reading circuit for reading address information from the read data in accordance with the address sync mark detection signal and the read clock signal; and

a first ID decision circuit for generating a read address read from the address information and a decision result indicating whether the read address is normal in accordance with the read clock signal;

a plurality of delay circuits for generating a plurality of delay clock signals having different phases from one another from the read clock signal;

a plurality of second ID reading apparatuses which operate in accordance with the plurality of delay clock signals, the second ID reading apparatuses including:

a second address sync mark detection circuit for detecting the address sync mark from data read from the header portion in accordance with an associated one of the plurality of delay clock signals and generating an address sync mark detection signal;

a second ID reading circuit for reading address information from the read data in accordance with the address sync mark detection signal and the associated one of the plurality of delay clock signals; and

a second ID decision circuit for generating a read address read from the address information and a decision result indicating whether the read address is normal in accordance with the associated one of the plurality of delay clock signals; and

a selector circuit which receives a plurality of read addresses and a plurality of decision results from the first reading apparatus and the plurality of second reading apparatuses and selects a best read address and decision result from thereamong.

7. The apparatus according to claim 6, wherein the selector circuit selects the best read address from the plurality of read addresses based on which read address is in a majority among the read addresses.

8. The apparatus according to claim 7, wherein the selector circuit includes an address comparing circuit for deciding which read address matches the greatest number of other read addresses among the plurality of read addresses; and

an output circuit for outputting the read address

having the greatest number of matches and a decision result corresponding to the read address having the greatest number of matches based on an output decision from the address comparing circuit.

9. The apparatus according to claim 6, wherein each of the first and second delay circuits includes at least one buffer circuit for delaying the read clock signal.

10. The apparatus according to claim 9, wherein the number of the at least one buffer circuit of the first delay circuit differs from that of the second delay circuit.

11. The apparatus according to claim 6, wherein each of the first and second delay circuits includes:

a frequency multiplier for multiplying a frequency of the read clock signal; and

flip-flop circuits connected in series to one another, to each of which a multiplied clock signal is provided from the frequency multiplier and to a first stage of which the read clock signal is provided.

12. A method of reading data from a disk, the method comprising:

generating a read clock signal based on rotational speed and recording density of the disk;

reading address information from a header portion recorded in each sector of the disk in accordance with the read clock signal; and

reading data recorded in a data portion of each sector based on the address information.

13. The method according to claim 12, wherein said generating the read clock signal includes computation of a

frequency of the read clock signal in accordance with the rotational speed and recording density of the disk.

14. The method according to claim 12, further comprising generating a plurality of delay clock signals having different phases from one another from the read clock signal.

15. The method according to claim 14, wherein said reading the address information includes reading of the address information at different timings in accordance with the plurality of delay clock signals.

16. The method according to claim 15, further comprising selecting a best read address and error detection result from the read addresses read at different timings and error detection results for the read addresses.

17. A method of reading data from a disk, the method comprising:

generating a read clock signal based on rotational speed and recording density of the disk;

generating a plurality of delay clock signals having different phases from one another from the read clock signal;

reading address information recorded in a header portion of each sector of the disk in accordance with the read clock signal;

reading the address information in accordance with the plurality of delay clock signals;

selecting the address information which has the greatest number of matches from the address information read at different timings; and

reading the data based on the selected address

information.

18. The method according to claim 17, wherein said generating the read clock signal includes computation of a frequency of the read clock signal in accordance with the rotational speed and recording density of the disk.